IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A semiconductor memory device comprising:

a memory cell array including at least a first area and a second area~~, which stores cell data~~;

a data input circuit located closer to the first area than the second area, to which ~~the~~ cell data stored in the memory cell array is input;

an error correction circuit which generates parity data for error correction from the cell data input to the data input circuit; and

a control circuit which writes the parity data into the first area and writes the cell data into the second area at a time of a writing operation ~~stores the parity data in the first area~~.

Claim 2 (Original): The semiconductor memory device according to claim 1, wherein the memory array includes a first memory unit and a second memory unit having the first area and the second area, respectively.

Claim 3 (Original): The semiconductor memory device according to claim 1, wherein the memory array includes a first data line connected to the first area and a second data line connected to the second area.

Claim 4 (Original): The semiconductor memory device according to claim 3, further comprising a switch between the first data line and the second data line.

Claim 5 (Original): The semiconductor memory device according to claim 1, wherein the memory array includes a common data line connected to both the first area and the second area.

6. (Canceled)

Claim 7 (Currently Amended): The semiconductor memory device according to claim 1 [[6]], wherein the control circuit stores both the parity data and the cell data in the first area and ~~store~~ stores the cell data not including the parity data in the second area.

Claim 8 (Currently Amended): The semiconductor memory device according to claim 1 [[6]], wherein the memory array includes at least a first memory unit and a second memory unit each having the first area and the second area.

Claim 9 (Original): The semiconductor memory device according to claim 8, wherein the first memory unit has a first data line connected to the first area and a second data line connected to the second area, and the second memory unit has a first data line connected to the first area and a second data line connected to the second area.

Claim 10 (Original): The semiconductor memory device according to claim 9, wherein the first data line and the second data line are electrically connected to or disconnected from each other by a selection switch.

Claim 11 (Original): The semiconductor memory device according to claim 8, wherein the first memory unit and the second memory unit each have a common data line connected to both the first area and the second area.

Claim 12 (Original): The semiconductor memory device according to claim 1, wherein the memory array includes at least a first memory unit and a second memory unit each having the first area and the second area, and the semiconductor memory device further comprises a switching circuit which stores the parity data in the first area of one of the first memory unit and the second memory unit.

Claim 13 (Original): The semiconductor memory device according to claim 1, further comprising a data compensating circuit which error-corrects the cell data stored in the memory array using the parity data stored in the first area.

Claim 14 (Original): The semiconductor memory device according to claim 1, wherein a size of the first area is equal to or smaller than that of the second area.

Claims 15–17 (Canceled).

Claim 18 (New): The semiconductor memory device according to claim 1, wherein the control circuit simultaneously activates the first area and the second area.

Claim 19 (New): The semiconductor memory device according to claim 2, wherein the control circuit simultaneously activates the first area of the first memory unit and the second area of the second memory unit.

Claim 20 (New): The semiconductor memory device according to claim 2, wherein the control circuit simultaneously activates the second area of the first memory unit and the first area of the second memory unit.